Docket No.: GR 98 P 2661 D

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Manfred Engelhardt
Div. of Applic. No.	:	09/816,923, filed March 23, 2001
Div. filed	:	August 22, 2003
Title	:	Method of Producing an Integrated Circuit Configuration
Examiner	:	Alexander O. Williams Group Art Unit: 2826

INFORMATION DISCLOSURE STATEMENT

Hon. Commissioner for Patents,
Alexandria, VA 22313-1450

S i r :

In accordance with 37 C.F.R. 1.98, the following patents and/or publications are cited herewith:

U.S. Patent No. 5,308,793 (Taguchi et al.), dated May 3, 1994;

U.S. Patent No. 5,612,254 (Mu et al.), dated March 18, 1997;

Published European Patent Application No. EP 0 798 778 A2 (Inohara et al.), dated October 1, 1997;

International Search Report dated March 7, 2000;

International Preliminary Examination Report dated December 21, 2000.

The above-mentioned references were cited in an *Information Disclosure Statement* filed July 30, 2002, in parent application No. 09/816,923.

Published, European Patent Application No. EP 0 892 428 A2 (Nguyen et al.), dated January 20, 1999;

"A High Performance 3.97μm^2 CMOS SRAM Technology Using Self-Aligned Local Interconnect and Copper Interconnect Metallization" (Woo et al.), 1998 Symposium on VLSI Technology Digest of Technical Papers, pp. 12-13;

"A High-Performance Sub-0.25 μm CMOS Technology with Multiple Thresholds and Copper Interconnects" (Su et al.), 1998 Symposium on VLSI Technology Digest of Technical Papers, pp. 18-19.

The above-mentioned references were cited in an *Information Disclosure Statement* filed August 19, 2002, in parent application No. 09/816,923.

U.S. Patent No. 5,966,634 (Inohara et al.), dated October 12, 1999;

U.S. Patent No. 6,150,272 (Liu et al.), dated November 21, 2000.

The above-mentioned references were cited in an Office Action dated September 19, 2002, in parent application No. 09/816,923.

U.S. Patent No. 6,136,682 (Hegde et al.), dated October 24, 2000;

U.S. Patent No. 6,197,688 B1 (Simpson), dated March 6, 2001;

U.S. Patent No. 6,221,780 B1 (Greco et al.), dated April 24, 2001;

U.S. Patent No. 6,251,772 B1 (Brown), dated June 26, 2001;

U.S. Published Patent Application US 2002/0019131 A1 (Ohtsuka et al.), dated February 14, 2002;

U.S. Published Patent Application US 2002/0098673 A1 (Yeh et al.), dated July 25, 2002.

The above-mentioned references were cited in an Office Action dated April 4, 2003, in parent application No. 09/816,923.

U.S. Patent No. 6,472,304 B2 (Chittipeddi et al.), dated October 29, 2002

U.S. Published Patent Application US 2002/0005582 A1 (Nogami et al.), dated January 17, 2002;

U.S. Published Patent Application US 2002/0000665 A1 (Barr et al.), dated January 3, 2002.

The above-mentioned references were cited in an Office Action dated July 17, 2003, in parent application No. 09/816,923.

Respectfully submitted,

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For Applicants

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FORM PTO-1449 (SUBSTITUTE) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT (37 CFR 1.98(b))	Attorney Docket No.: GR 98 P 2661 P D Divisional of Applic. No. 09/816,923 Applicant Manfred Engelhardt Filing Date of Divisional August 22, 2003 Group Art Unit 2826

EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
	A	5,308,793	05/94	Taguchi et al.			
	B	5,612,254	03/97	Mu et al.			
	C	5,966,634	10/99	Inohara et al.			
	D	6,150,272	11/00	Liu et al.			
	E	6,136,682	10/00	Hegde et al.			
	F	6,197,688 B1	03/01	Simpson			
	G	6,221,780 B1	04/01	Greco et al.			
	H	6,251,772 B1	06/01	Brown			
	I	6,472,304 B2	10/02	Chittipeddi et al.			

FOREIGN PATENT DOCUMENT

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES	TRANSL. NO
	J	EP 0 798 778 A2	10/97	Europe				
	K	EP 0 892 428 A2	01/99	Europe				
	L							
	M							
	N							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

		"A High Performance 3.97μm^2 CMOS SRAM Technology Using Self-Aligned Local Interconnect and Copper Interconnect Metallization" (Woo et al.), 1998 Symposium on VLSI Technology Digest of Technical Papers, pp. 12-13.
		"A High-Performance Sub-0.25 μm CMOS Technology with Multiple Thresholds and Copper Interconnects" (Su et al.), 1998 Symposium on VLSI Technology Digest of Technical Papers, pp. 18-19.

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	A	US 2002/0098673 A1	07/02	Yeh et al.			
	B	US 2002/0005582 A1	01/02	Nogami et al.			
	C	US 2002/0000665 A1	01/02	Barr et al.			
	D	US 2002/0019131 A1	02/02	Ohtsuka et al.			
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	L							
	M							
	N							

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